Tutorial on Word-Level Model Checking

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Abstract—In SMT bit-vectors and thus word-level reasoning is common and widely used in industry. However, it took until 2019 that the hardware model checking competition started to use word-level benchmarks. Reasoning on the word-level opens up many possibilities for simplification and more powerful reasoning. In SMT we do see advantages due to operating on the word-level, even though, ultimately, bit-blasting and thus transforming the word-level problem into SAT is still the dominant and most important technique. For word-level model checking the situation is different. As the hardware model checking competition in 2019 has shown bit-level solvers are far superior (after bit-blasting the model through an SMT solver though). On the other hand word-level model checking shines for problems with memory modeled with arrays. In this tutorial we revisit the problem of word-level model checking, also from a theoretical perspective, give an overview on classical and more recent approaches for word-level model checking, and discuss challenges and future work.

The tutorial covered material from the following papers.

REFERENCES


[12] ——, “Word level bitwidth reduction for unbounded hardware model checking, and then discuss challenges and future work. On the other hand word-level model checking shines for problems with memory modeled with arrays. In this tutorial we revisit the problem of word-level model checking, also from a theoretical perspective, give an overview on classical and more recent approaches for word-level model checking, and discuss challenges and future work. The tutorial covered material from the following papers.

REFERENCES


World-Level Modelling

- bit-precise reasoning: **bit-vector** as basic modelling element

thus in essence SMT theory QF_BV of **bit-vectors**

- sorts: bit \( \mathbb{B} = \{0, 1\} \) bit-vector \( \mathbb{B}^w \)
- constants: \( 65_{10} \) decimal \( \; 00100011_2 \) binary \( \; 111\ldots111 \) (unary)
- variables: declared as \( b[1] \) and \( x[32] \) \( \text{bool } b, x[32]; \)
- comparison: \( =, \neq, <, \leq \) (signed and unsigned), …
- bit-wise operators: \( \sim, -, \land, \lor, \oplus, \ldots \) shifting operators: shift, rotate …
- arithmetic operators: \( +, -, *, /, \ldots \) string operators: slicing, append, extend, …

plus array theory QF_ABV to model memory main memory, caches, etc.

- sorts: array \( \mathbb{B}^r[2^d] = (\mathbb{B}^d \to \mathbb{B}^r) = \mathbb{B}^{r2^d} = \mathbb{B}^{r \cdot 2^d} \)
- constants: \( ? \) zero, range initializers, lambdas, quantifiers, …
- variables: declared as \( c[64][1024] \) \( 8\text{KB cache } \) \( m[8][2^{64}] \) main memory

\[
\text{(declare-fun c () (Array (_ BitVec 10) (_ BitVec 64)))}
\text{(declare-fun m () (Array (_ BitVec 64) (_ BitVec 8)))}
\]
- operators: read, write (update) select, store
Sequential Modelling = State Machines / Kripke Structures / Automata

- use “logic” (e.g., bit-vector formulas) to describe sequential semantics symbolically

- Kripke structure flavor  
  - think "SMV"
  - initialization and (total) transition relation
  - non-deterministic modelling thus inputs are part of the state
  - still usually variable based: state space = possible variable assignments
  - constraints (invariants / fairness) and properties (temporal logic)

- automata or circuit flavor  
  - think "Verilog" or AIGER on the bit-level
  - initialization and transition function
  - partial initialization important in AIGER
  - separate variables for inputs and states
  - non-determinism modelled with inputs "⋯ = *;" in SLAM, oracle / Choueka construction
  - constraints, properties and explicit outputs for simple compositional semantics
  - clear semantics close to actual HW / SW

- thus in summary we prefer the second “functional” view as in AIGER and BTOR
  - also gives a faster and simpler to implement model checker [JussilaBiere’07]
AIGER

- **bit-level** (propositional) functional model checking format
- bootstrapped first hardware model checking competition (HWMCC’07)
- witness / trace format, tool set for simulation / witness checking, splitting, unrolling …
- simple and clean semantics, common denominator of model checkers [Biere’07]
- constraints, more general properties and synthesis support [BiereHeljankoWieringa’11]
- now supported by many HW tools as (binary) exchange format (such as ABC)
- AIG means And-Inverter Graph (formulas with AND and NOT only)
- used since 2007 in the hardware model checking competition (HWMCC) [Cabodi et.al. : HWMCC’14] [BiereVanDijkHeljanko’17]
- collected and selected benchmark sets used in many papers

CAV’07 Berlin
CAV’10 FLOC’10 Edinburgh
FMCAD’12 Cambridge
CAV’14 FLOC’14 Vienna
FMCAD’17 Vienna
FMCAD’20 Virtual

CAV’08 Princeton
FMCAD’11 Austin
FMCAD’13 Portland
FMCAD’15 Austin
FMCAD’19 San Jose
AIGER

4-bit adder

toggle flip-flop with enable & reset
- **BTOR 1.0** [BrummayerBiereLonsing’09]
  - word-level generalization of the initial AIGER format from 2007 (ASCII version)
  - supports bit-vectors and arrays (again quantifier-free formulas only)
  - sequential functional extensions as in AIGER

- **BTOR 2.0** [NiemetzPreinerWolfBiere’18]
  - resumed word-level motivated by open flows (Yosys) and open cores (RISC-V)
  - incorporated new AIGER 1.9 features from 2011
  - witness format
  - new tools:
    - witness checker / simulator
    - bounded model checker
    - new bit-blaster on top of Boolector’s bit-blaster [Preiner’2019]
  - still lacking: fuzzer, delta debugger, bit-blasting of arrays
  - initialization of arrays still tricky
  - used in HWMCC’19 and HWMCC’20
BTOR Model Example

```plaintext
1 sort bitvec 1
2 sort bitvec 3
3 zero 2
4 state 2 cnt \{ cnt = 0 \}
5 init 2 4 3
6 input 2 in
7 add 2 4 6 \{ cnt' = cnt + in \}
8 next 2 4 7
9 ones 2
10 eq 1 4 9 \{ bad : (cnt == 7) \}
11 bad 10
12 constd 2 3
13 ulte 1 6 12 \{ in \leq 3 \}
14 constraint 13
```

Witness Example

```
sat
b0
#0
@0
0 011 in@0
@1
0 010 in@1
@2
0 010 in@2
@3
0 000 in@3
```

⟨num⟩ ::= positive unsigned integer (greater than zero)
⟨uint⟩ ::= unsigned integer (including zero)
⟨string⟩ ::= sequence of whitespace and printable characters without '\n'
⟨symbol⟩ ::= sequence of printable characters without 'n'
⟨comment⟩ ::= ';' ⟨string⟩
⟨nid⟩ ::= ⟨num⟩
⟨sid⟩ ::= ⟨num⟩
⟨const⟩ ::= 'const' ⟨sid⟩ [0-1]+
⟨constd⟩ ::= 'constd' ⟨sid⟩ ['\-']⟨uint⟩
⟨consth⟩ ::= 'consth' ⟨sid⟩ [0-9a-fA-F]+
⟨input⟩ ::= ('input' | 'one' | 'ones' | 'zero') ⟨sid⟩ | ⟨const⟩ | ⟨constd⟩ | ⟨consth⟩
⟨state⟩ ::= 'state' ⟨sid⟩
⟨bitvec⟩ ::= 'bitvec' ⟨num⟩
⟨array⟩ ::= 'array' ⟨sid⟩ ⟨sid⟩
⟨node⟩ ::= ⟨sid⟩ 'sort' (⟨array⟩ | ⟨bitvec⟩)  
  | ⟨nid⟩ (⟨input⟩ | ⟨state⟩)  
  | ⟨nid⟩ ⟨opidx⟩ ⟨sid⟩ ⟨nid⟩ ⟨uint⟩ [⟨uint⟩]  
  | ⟨nid⟩ ⟨op⟩ ⟨sid⟩ ⟨nid⟩ [⟨nid⟩] [⟨nid⟩]  
  | ⟨nid⟩ ('init' | 'next') ⟨sid⟩ ⟨nid⟩ ⟨nid⟩  
  | ⟨nid⟩ ('bad' | 'constraint' | 'fair' | 'output') ⟨nid⟩  
  | ⟨nid⟩ 'justice' ⟨num⟩ (⟨nid⟩ )+
⟨line⟩ ::= ⟨comment⟩ | ⟨node⟩ [⟨symbol⟩] [⟨comment⟩]
⟨btor⟩ ::= ( ⟨line⟩'\n' )+
BTOR2 Witness Format

⟨binary-string⟩ ::= [0-1]+
⟨bv-assignment⟩ ::= ⟨binary-string⟩
⟨array-assignment⟩ ::= [' ' ⟨binary-string⟩ '] ' ⟨binary-string⟩
⟨assignment⟩ ::= ⟨uint⟩ ( ⟨bv-assignment⟩ | ⟨array-assignment⟩ ) [ ⟨symbol⟩ ]
⟨model⟩ ::= ( ⟨comment⟩ '\n' | ⟨assignment⟩ '\n' )+
⟨state part⟩ ::= #' ⟨uint⟩ '\n' ⟨model⟩
⟨input part⟩ ::= '@' ⟨uint⟩ '\n' ⟨model⟩
⟨frame⟩ ::= [ ⟨state part⟩ ] ⟨input part⟩
⟨prop⟩ ::= ('b' | 'j') ⟨uint⟩
⟨header⟩ ::= 'sat\n' ( ⟨prop⟩ )+ '\n'
⟨witness⟩ ::= ( ⟨comment⟩ '\n' )+ | ⟨header⟩ ( ⟨frame⟩ )+ '.

https://github.com/Boolector/btor2tools
Another Example Modelling a C program

```c
#include <assert.h>
#include <stdio.h>
#include <stdlib.h>
#include <stdbool.h>

static bool read_bool () {
    int ch = getc (stdin);
    if (ch == '0') return false;
    if (ch == '1') return true;
    exit (0);
}

int main () {
    bool turn; // input
    unsigned a = 0, b = 0; // states
    for (;;) {
        turn = read_bool ();
        assert (!(a == 3 && b == 3));
        if (turn) a = a + 1;
        else b = b + 1;
    }
}
```

1 sort bitvec 1
2 sort bitvec 32
3 input 1 turn
4 state 2 a
5 state 2 b
6 zero 2
7 init 2 4 6
8 init 2 5 6
9 one 2
10 add 2 4 9
11 add 2 5 9
12 ite 2 3 4 10
13 ite 2 -3 5 11
14 next 2 4 12
15 next 2 5 13
16 constd 2 3
17 eq 1 4 16
18 eq 1 5 16
19 and 1 17 18
20 bad 19
Application Specific Sequential Word-Level Formats

- Hardware description languages (HDL): (System)-Verilog, System-C, VHDL, ...
  - “what you check is what you get”
  - usually have (very) complex semantics and undefined behaviour
  - Yosys, Reveal, Enhanced ABC, commercial model checkers

- Software languages: C, Java, JVM, GraalVM, LLVM, assembler, ...
  - “what you check is what you get”
  - usually have complex semantics and undefined behaviour
  - “Competition on Software Verification” SV-Comp

- Application specific languages problematic
  - hard to reuse solver / checker technology
  - QF_BV is pretty successful in both HW and SW applications
  - encode “undefinedness” precisely is better
  - same should apply to model checking

- but: “v2c – A Verilog to C translator ”

[MukherjeeTautschnigKroening’16] [MukherjeeSchrammelKroeningMelham’16]
Other Generic Word-Level Model Checking Formats

- **UCLID** [BryantLahiriSeshia]
  - early SMT solving (UF, lambdas, memory) targeting processor verification
  - bounded model checking in essence (manual inductive verification)

- **SAL** from SRI [DeMouraOwreShankar’03] Yices [Duherte’14]
  - focus was originally on infinite systems
  - sofar not-much interest in bit-precise reasoning

- **constrained horn clauses** \(\mu Z\) [HoderBjornerDeMoura’11]
  - basically extends an SMT solver (Z3) with (second order) least fix-points
  - active community: workshops, competition, …
  - sofar not-much interest in bit-precise reasoning

- **VMT** nuXmv [CAV’14] Verilog2SMV [DATE’16] from FBK IRST in Trento
  - SMTLIB with annotations to mark initialization and transition predicates
  - built around (nu)SMV using MathSAT as word-level engine
  - actively supports bit-vectors

- related ”Model Checking Competition” (MCC) has Petri nets models (in PNML)

- “classical” protocol modelling languages: Promela (SPIN), Murphi, …
Bit-Blasting Explodes

- show *commutativity of bit-vector addition* for bit-width 1 million:

  (set-logic QF_BV)
  (declare-fun x () (_ BitVec 1000000))
  (declare-fun y () (_ BitVec 1000000))
  (assert (distinct (bvadd x y) (bvadd y x)))

- size of SMT2 file: **138 bytes**

- bit-blasting with our SMT solver Boolector
  - rewriting turned off
  - except structural hashing
  - produces AIGER circuits of file size **103 MB**

- Tseitin transformation leads to CNF in DIMACS format of size **1 GB**
Complexity Classification Results for Bit-Vector Logics

our results from [KovásznaiFröhlichBiere-SMT’12] paper extended version in our TOCS’16 article

<table>
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<td></td>
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<tr>
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</tr>
<tr>
<td>unary</td>
<td>NP QF_{BV1} obvious</td>
<td>NP QF_{UFBV1} Ackermann</td>
<td>PSACE BV1 [TACAS’10] NEXPTIME UFBV1 [FMCAD’10]</td>
</tr>
<tr>
<td>binary</td>
<td>NEXPTIME QF_{BV2} [SMT’12]</td>
<td>NEXPTIME QF_{UFBV2} [SMT’12]</td>
<td>AEXP(poly) BV2 [JonášStrejček-IPL’18] 2NEXPTIME UFBV2 [SMT’12]</td>
</tr>
</tbody>
</table>

QF = “quantifier free”    UF = “uninterpreted functions”    BV = “bit-vector logic”
BV1 = “unary encoded bit-vectors”    BV2 = “binary encoded bit-vectors”
AIGER problems are PSPACE complete
  - since “symbolic reachability” is PSPACE complete [Savitch’70]

now assume (for instance) sequential BTOR 2.0 as input
  - without arrays but sequential problems (model checking)
    - unary encoding (or bit-width as fixed parameter): PSPACE complete
    - binary encoding: EXSPACE complete [KovasznaiVeithFröhlichBiere’MFCS14]
  - with arrays and sequential problems (model checking)
    - unary encoding:
      - ? EXPSPACE complete?
    - binary encoding:
      - ? 2EXPSPACE complete?

benefits of complexity characterizations
  - gives hints what solvers (SAT, SMT, AIGER) can be used as oracles
  - and how many times they have to be called
  - sometimes gives restricted classes PSPACE sub-class of QF_BV2
Why do we want to do word-level model checking?

- use word-level “structure” for rewriting / simplification
  - allows (shallow) arithmetic reasoning as in the complexity example
  - word-level local search [NiemetzPreinerBiere'16/17] [NiemetzPreiner'20]
- make full use of functional representation
  - global substitution pass instead of congruence closure
  - CNF preprocessing lacks some benefits of circuit representations
  - bit-level circuit intermediate formats (thus bit-level rewriting)
- BDD / SAT / SMT / cut sweeping to eliminate equivalent expressions

- data and memory abstraction
  - bit-blasting of arithmetic expensive \*_{32} has 8000 AIG nodes, \*_{64} has 32 000
  - protocols only “move data around”: bit-precise reasoning redundant
  - properties often argue about some “reads” and “writes” only
  - bit-blasting memory is often impossible \( m_{32}[8][2^{32}] \) \( m_{64}[8][2^{64}] \)

- sequential and non-sequential rewriting and abstraction techniques
Eager Data Abstraction

- 1-bit abstractions
  - verify sorting using only “compare & swap” on 0/1 input zero-one principle [Knuth’73]
  - data independence of protocols [Wolper’86]

- small domain encoding part of Ackermann’s reduction
  - if you only compare $n$ variables then interpret them on the domain $0, \ldots, n-1$
  - reduce those variables to bit-width $\lceil \log n \rceil$
  - eager translation to SAT possible [PnueliRodehShtrichmanSiegel’99]
  - plain bit-vectors [Johannsen’01/02], model checking [HojatiBrayton’95] [Bjesse’08]
  - need to “slice” bit-vectors in HW to have compatible widths next state functions too
  - can use different domain size for each “cluster” of compared variables

- abstract uninterpreted functions (UF) through Ackermann eagerly transformation
  - extends to memories / arrays (exponentially) eliminate read & write as in UCLID
  - works for plain bit-vectors (thus BMC) but then lazy SMT (QF_AUFBV) is better [BurchDill’96] [VelevBryantJain’97] [ManoliosSrinivasanVroon’06] [GanaiGuptaAshar’04/05]
  - model checking requires to change properties [Bjesse’08/09] [German’11]
Lazy Data Abstraction

- akin to “lazy SMT” or CEGAR / Localization
- for instance replace expensive operations (multiplication) with UF
  - abstraction refinement loop using SMT  
    [AndrausLiffitonSakkalah’06/08]
  - conservative: if abstracted model passes property then original passes it too
  - spurious counter example: refine \( mult(x,y) \) to \( (x = 0 ? 0 : mult(x,y)) \)
  - refinement can make use of cores or MUS
- combine with IC3 / PDR  
  [LeeSakallah’14] [GoelSakallah’19/20]
  - predicate abstraction  
    existing predicates, new predicates?
  - syntax guided abstraction  
    equality between existing expressions, new expressions?
- how to interpolation into the mix is still unclear
  - bit-vectors [Griggio’16] [BackemanRümmerZeljic’18] [OkudonoKing’20]  
    arrays?
- also still needs to be combined with successful bit-level techniques
  - sweeping / temporal decomposision / retiming
  - local search / simulation
Challenges

- benchmarks: Yosys, open cores, RISC-V already helped a lot, but need more!
- apply HW word-level model checkers to SW (from SV-COMP) or vice versa
- symbolic execution of both SW and HW
  - modelling (slices of) programs linearly in a word-level model
  - “Selfie” by Christoph Kirsch has a BTOR2 model of RISC-U
- smart contracts
  - bit-precise semantics lends itself to word-level models
  - as discussed in invited SMT’20 talk by Mooly Sagiv
- certificates:
  - UNSAT proofs in SAT very useful
  - certificates for (passing properties) in AIGER
  - certificates for UNSAT proofs in QF_BV
  - combine to provide word-level certificates
  - make word-level model checkers faster than bit-level checkers ⇒ HWMCC’20?