Boolector 0.4

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- SMT solver

- Theories
  - QF_BV
  - QF_AUFBV

- Model Checker for safety properties
  - Sequential and synchronous circuits with registers and memories
  - BTOR
• C

• Term-level rewriting
  – Bounded rewriting
  – **Substitution of variables**
  – **Substitution of slices** on bit-vector variables
  – Normalization of $\text{bvadd}$ and $\text{bvmul}$ on demand
  – Local two level rewriting
  – Linear equation solver
• And-Inverter Graph Synthesis
  
  – Each expression is synthesized into AIG
    
    * For example `bvMul` is synthesized into AIG multiplier circuit
    
    * Local two level AIG rewriting  [BrummayerBiere06]
  
  – AIG is encoded into CNF
  
  – PicoSAT is used as SAT solver

• **Lemmas on demand** for QF_AUFBV  [BrummayerBiere08]
  
  – Propagation-based fix-point algorithm
  
  – Incremental formula refinement