Hardware Model Checking Competition 2017

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The Hardware Model Checking Competition (HWMCC) 2017 affiliated to the International Conference on Formal Methods in Computer Aided Design (FMCAD) in 2017 in Vienna was the 9th competitive event for hardware model checkers we organized. After HWMCC'15 affiliated with FMCAD'15 in Austin, the competition took a break in 2016.

The competition has its roots in the model checking community with focus on hardware verification, a former central theme in International Conference on Computer-Aided Verification (CAV) and the first three incarnations of the competition in 2007, 2008 and 2010 were affiliated with CAV. This topic is now more at home at FMCAD, the primary place for research in formal methods for hardware. Accordingly the hardware model checking competition stays with FMCAD (2011,2012,2013,2015,2017) except when CAV is part of the Federated Logic Conference (FLoC) as in 2014 [4].

The goal in organizing this competition is to keep up the driving force in improving hardware model checkers. We also want to motivate implementors to present their work to a broader audience. Another important objective is to collect realistic benchmarks and to make them available to the research community. Both academia and industry is invited to submit solvers and benchmarks. Competiting model checkers have to solve benchmarks in the AIGER format [2], [3].

The competition in 2017 had multiple tracks. The most important track was the single safety property track (SINGLE). As in previous years we also had a (single) liveness property track (LIVE), and a deep bound track (DEEP), but no multiple property track. The winner of the deep bound track received an award of $500 sponsored by Oski Technology.

The tracks were run in the same way as in the previous four incarnations of the competition, except that we were using our new cluster running Ubuntu 16.04.2 64 bit. Each cluster node had two Intel(R) Xeon(R) CPU E5-2620 v4 @ 2.10GHz CPUs and 128 GB of main memory.

Each solver had full access to both processors on one node, thus combined 16 cores (32 virtual cores) and 128 GB of main memory. Accordingly a memory limit of 120GB was enforced. As in the last competition in 2015 affiliated to FMCAD'15 we were further using a time limit of 1 hour of wall clock-time.

Also as before the number of submissions was restricted to at most two model checkers per submitter and model checkers were required to produce witnesses in the SINGLE track. These witnesses were checked by the AIGSIM tool, which is part of the AIGER tools [1].

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Except for the new hardware, competition rules, as well as input and output formats [2] did not change compared to previous competitions. As starting with HWMCC'12 model checkers competing in the DEEP bound track were requested to print the bounds reached during running in the SINGLE track. In the SINGLE track model checkers were required to print witnesses traces if a bad state was claimed to be reachable. These witnesses serve as certificates for satisfiable bad state properties and were checked for correctness.

Again as in HWMCC'14 and HWMCC'15, in order to avoid glitches in interpreting the format, the SINGLE track only used AIGER pre 1.9 single property benchmarks [2], with the single bad state property encoded as an output (MILOA header with O = 1). All latches were assumed to be initialized implicitly to zero as it is the default in the pre 1.9 AIGER format [2].

There was no change in the LIVE track which of course used the AIGER 1.9 format [3] nor in the DEEP track. Solvers intended to participate in the DEEP track were run in the SINGLE track and were expected to print reached bounds as in previous years (see for instance HWMCC'12).

In the previous competition HWMCC'15 we were proposing to completely switch to the AIGER 1.9 format [3] (also in the SINGLE track), add back the multiple property track, provide support for fuzzing and delta-debugging, and last but not least to establish a word-level track. However, due to lack of resources, we had to postpone these changes again.

References

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