Arithmetic Verification Problems
Submitted to the SAT Race 2019

Daniela Kaufmann  Manuel Kauers  Armin Biere
Johannes Kepler University Linz

David Cok
Safer Software Consulting

MULTIPLIER MITERS
In the benchmark description of our arithmetic challenge problems [1] submitted to the SAT Competition 2016, we have mentioned that there is another source of multiplier designs, which we could not retrieve back then. These circuits described in [2] were used in [3] and then synthesized and translated to AIGs in our related work [4]. Furthermore, the corresponding web-service “Arithmetic Module Generator” for generating the circuits (in Verilog) became recently available again at [https://www.ecsis.riec.tohoku.ac.jp/topics/amg/]. For the SAT Race 2019 we generated AIG miters and encoded them into CNF for interesting bit-widths 10, 12 and 14, where SAT solvers not using algebraic reasoning start to have a hard time. These benchmarks compare pairwise several multipliers with different architectures and characteristics. We also considered unsigned multipliers and a few signed multipliers (these are all \(n \times n\) inputs to \(2n\) bits outputs multipliers where signedness makes a difference). We compare two signed architectures “2cbpwtcl” and “2csparrc” with prefix “eq2...” which gives 6 signed benchmarks for bit-widths 10,12,14. The 12 unsigned multiplier architectures we compare are bparcl, bparrc, bpcstk, bpdft, bptwcl, bptwrc, sparc, sparrc, spctbk, spdtlf, spwtcl, spwtrc for bit-widths 10,12 and 14, which gives 396 = 3 \(\times\) 12 \(\times\) 11 unsigned benchmarks (all with “eq...” but without “eq2”, “btor” nor “ktsb” in their name).

KARATSUBA MULTIPLICATION
As crafted benchmark we generated a bit-vector implementation of a single recursive step of the well-known Karatsuba multiplication algorithm. The implementation is then compared against a full multiplier of the same architecture (BTOR). We submitted only the three benchmarks “eqbtor10ktsb\{10,12,14\}*cnf” for bit-widths 10,12 and 14.

THE CRUX OF MULTIPLIER VERIFICATION
During our work on multiplier verification we came across the issue that within a single column of a multiplier circuit (producing a certain output bit) the sum of the partial products can be permuted in an arbitrary order. Since adding up these partial products within a column needs adders of logarithmic size this summation requires bit-vector reasoning. In different multipliers these adders are ordered and grouped differently, which we conjecture to be the “crux” of multiplier verification on the bit-level.

To capture this problem we generated benchmarks which add up \(n\) bits with two input adder trees in a random order and grouping. The input bits are zero extended to \(m\) bits, which is the minimum number such that \(2^m > n\). Then we generate two different random adder trees. Each tree consists of \(n - 1\) adders of bit-width \(m\). The outputs of the two trees are compared, which is getting hard for standard SAT solvers on the CNF level at around \(n = 30\) bits. We used 10 different seeds for \(n = 20, \ldots, 32\) and thus submitted 130 benchmarks “cruximiters\{20,...,32\}seed\{0-9\}.cnf”.

INTEGRAL OVERFLOW CHECK
In program analysis of code similar to the following C program, the overflow check might yield hard bit-vector problems:

```c
void *calloc (size_t a, size_t b) {
    if (((size_t)-1) / a < b) return NULL;
    return memset (malloc (a*b), 0, a*b);
}
```

Here is a corresponding SMT formula for this check

```smt
(set-logic QF_BV)
(declare-fun a () (_ BitVec 32))
(declare-fun b () (_ BitVec 32))
(assert
  (not (= (_ extract 63 32)
          (bvmul (_ zero_extend 32) a)
          (_ zero_extend 32) b))
  (_ bv0 32)))
(assert
  (bvuge (bvdiv (bvnor (_ bv0 32)) a) b))
```

This is for a 32-bit machine. We generated 29 instances for bit-widths 20 to 48 called “davidcokchallenge\{20,...,48\}.cnf”. This problem is getting hard around 36 bits.

REFERENCES

Supported by FWF, NFN Grant S11408-N23 (RiSE)