Introduction to Bounded Model Checking Armin Biere

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FATS Seminar

ETH Zürich, Switzerland

Wednesday, October 28, 2009

DavisPutnam'60: DP

CoudertMadre'89: Symbolic Reachability McMillan'03: Interpolation

DavisLogemannLoveland'62: DPLL Marques-SilvaSakallah'96: GRASP

Bryant'86: BDDs BiereArthoSchuppan'01: Liveness2Safety

Pnueli'77: Temporal Logic MoskewiczMadiganZhaoZhangMalik'01: CHAFF

McMillan'93: SMV

EenSorensson'03: MiniSAT

ClarkeEmerson'82: Model Checking BiereCimattiClarkeZhu'99: Bounded Model Checking

Kurshan'93: Localization

SheeranSinghStalmarck'00: *k* –Induction

QuielleSifakis'82: Model Checking

BallRajamani'01: SLAM

ClarkeEmersonSifakis: Turing Award 2007

EenBiere'05: SatELite

Holzmann'91: SPIN

GrafSaidi'97: Predicate Abstraction

Holzmann'81: On–The–Fly Reachability ClarkeGrumbergJahLuVeith'03: CEGAR

Peled'94: Partial-Order-Reduction

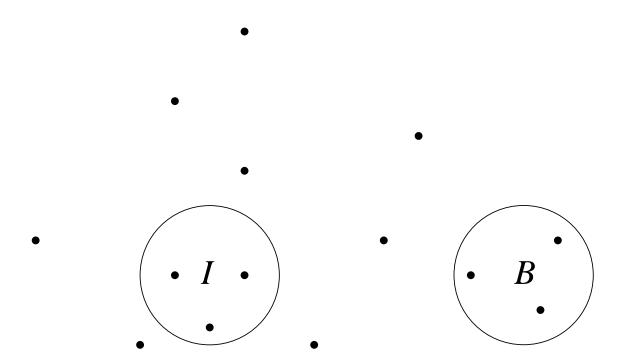
models:

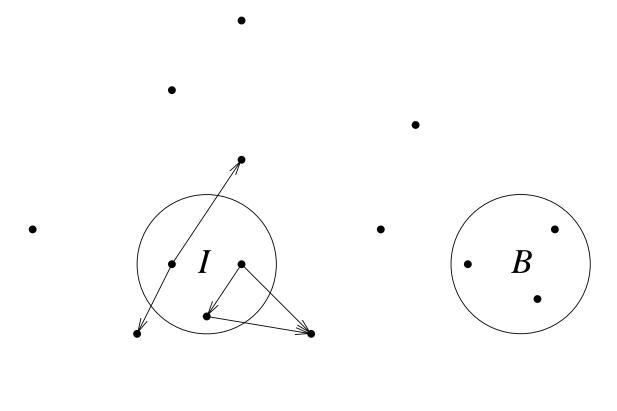
- finite automata, labelled transition systems
- often requires automatic/manual abstraction techniques

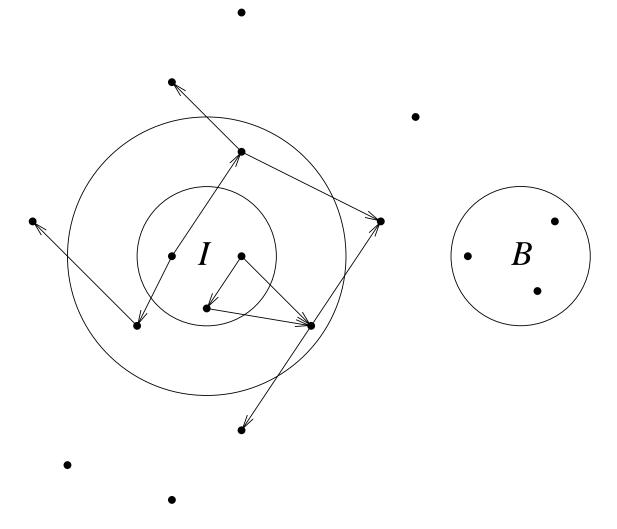
• properties:

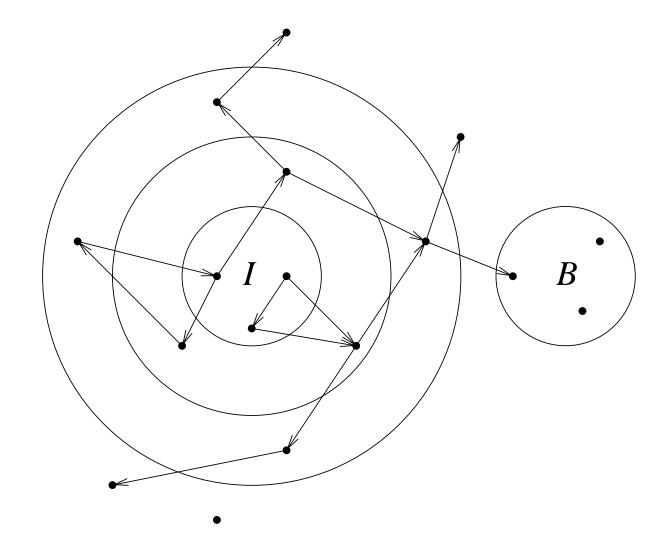
- mostly interested in partial properties
- specified in temporal logic: CTL, LTL, etc.
- safety: something bad should not happen
- liveness: something good should happen
- automatic generation of counterexamples

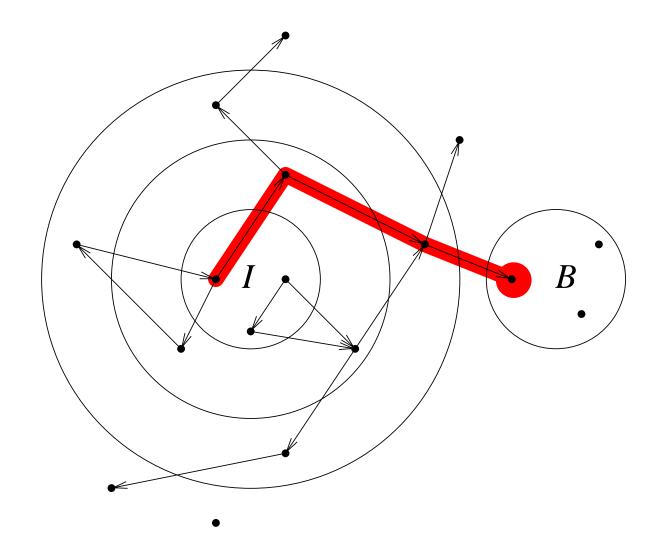
- set of states S, initial states I, transition relation T
- bad states *B* reachable from *I* via *T*?
- symbolic representation of T (ciruit, program, parallel product)
 - avoid explicit matrix representations, because of the
 - state space explosion problem, e.g. *n*-bit counter: |T| = O(n), $|S| = O(2^n)$
 - makes reachability PSPACE complete [Savitch'70]
- on-the-fly [Holzmann'81'] for protocols
 - restrict search to reachable states
 - simulate and hash reached concrete states

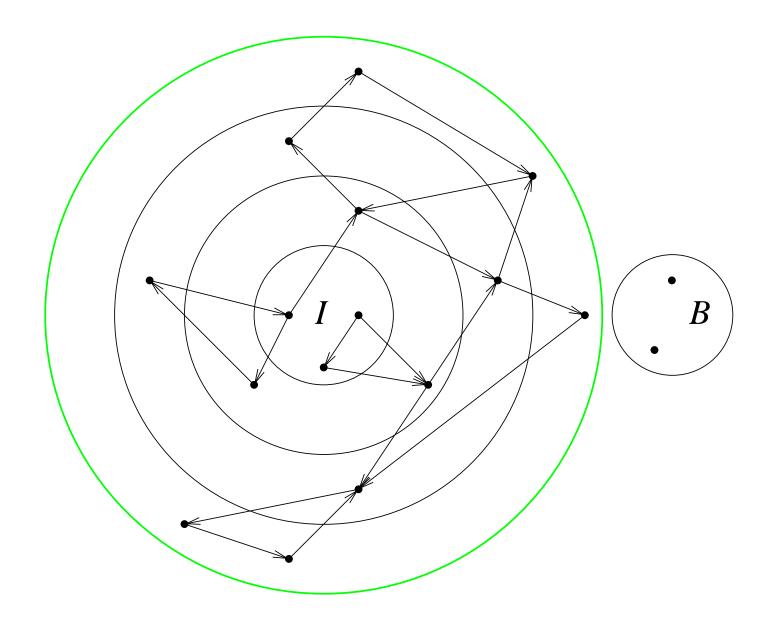








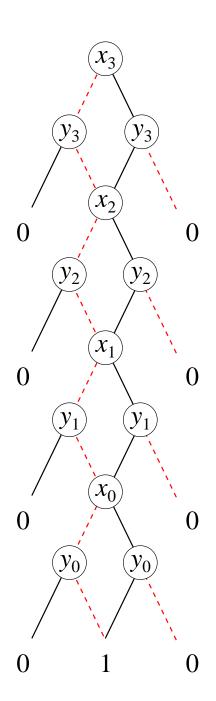




initial states I, transition relation T, bad states B

```
\underline{\text{model-check}}_{\text{forward}}^{\mu} (I, T, B)
     S_C = \emptyset; S_N = I;
     while S_C \neq S_N do
        if B \cap S_N \neq \emptyset then
           return "found error trace to bad states";
        S_C = S_N;
        S_N = S_C \cup \frac{Img(S_C)}{Img(S_C)};
     done;
     return "no bad state reachable";
```

- work with symbolic representations of states
 - symbolic representations are potentially exponentially more succinct
 - favors BFS: next frontier set of states in BFS is calculated symbolically
- originally "symbolic" meant model checking with BDDs [CoudertMadre'89/'90,BurchClarkeMcMillanDillHwang'90,McMillan'93]
- Binary Decision Diagrams [Bryant'86]
 - canonical representation for boolean functions
 - BDDs have fast operations (but image computation is expensive)
 - often blow up in space
 - restricted to hundreds of variables



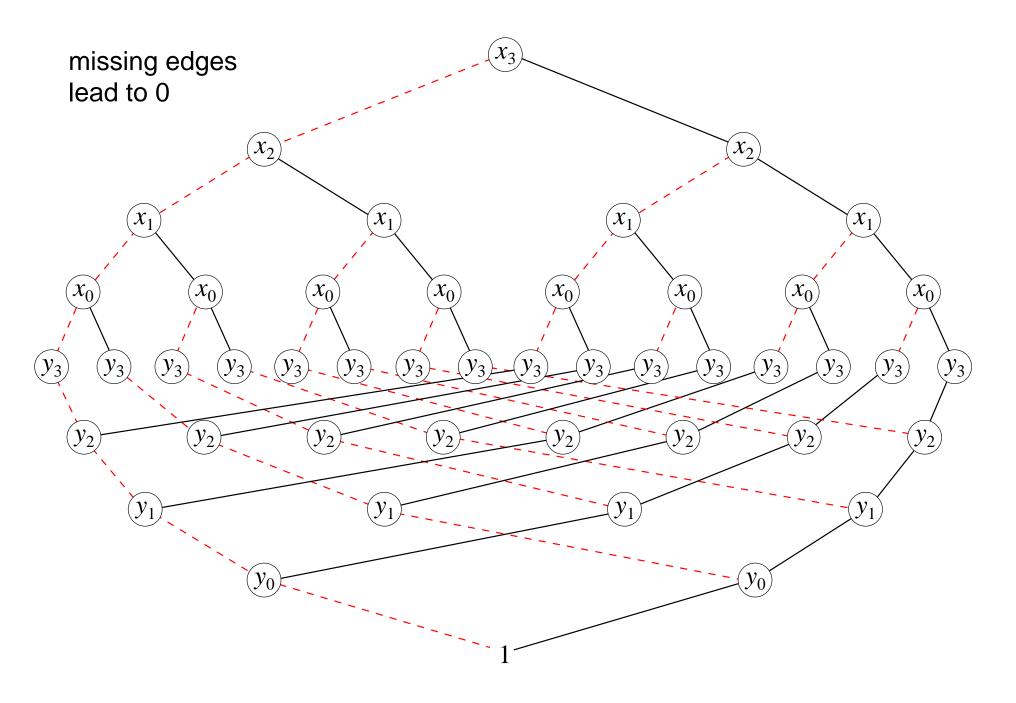
boolean function/expression:

$$\bigwedge_{i=0}^{n-1} x_i = y_i$$

interleaved variable order:

$$x_3 > y_3 > x_2 > y_2 > x_1 > y_1 > x_0 > y_0$$

comparison of two n-bit-vectors needs $3 \cdot n$ inner nodes for the interleaved variable order



0: continue?
$$S_C^0 \neq S_N^0 \quad \exists s_0[I(s_0)]$$

0: terminate?
$$S_C^0 = S_N^0 \quad \forall s_0[\neg I(s_0)]$$

0: bad state?
$$B \cap S_N^0 \neq \emptyset$$
 $\exists s_0[I(s_0) \land B(s_0)]$

1: continue?
$$S_C^1 \neq S_N^1 \quad \exists s_0, s_1[I(s_0) \land T(s_0, s_1) \land \neg I(s_1)]$$

1: terminate?
$$S_C^1 = S_N^1 \quad \forall s_0, s_1[I(s_0) \land T(s_0, s_1) \rightarrow I(s_1)]$$

1: bad state?
$$B \cap S_N^1 \neq \emptyset$$
 $\exists s_0, s_1[I(s_0) \land T(s_0, s_1) \land B(s_1)]$

2: continue?
$$S_C^2 \neq S_N^2 \quad \exists s_0, s_1, s_2[I(s_0) \land T(s_0, s_1) \land T(s_1, s_2) \land \neg (I(s_2) \lor \exists t_0[I(t_0) \land T(t_0, s_2)])]$$

2: terminate?
$$S_C^2 = S_N^2$$
 $\forall s_0, s_1, s_2[I(s_0) \land T(s_0, s_1) \land T(s_1, s_2) \rightarrow I(s_2) \lor \exists t_0[I(t_0) \land T(t_0, s_2)]]$

2: bad state?
$$B \cap S_N^1 \neq \emptyset$$
 $\exists s_0, s_1, s_2[I(s_0) \land T(s_0, s_1) \land T(s_1, s_2) \land B(s_2)]$

0: continue? $S_C^0 \neq S_N^0 \quad \exists s_0[I(s_0)]$

0: terminate? $S_C^0 = S_N^0 \quad \forall s_0[\neg I(s_0)]$

0: bad state? $B \cap S_N^0 \neq \emptyset$ $\exists s_0[I(s_0) \land B(s_0)]$

1: continue? $S_C^1 \neq S_N^1 = \exists s_0, s_1[I(s_0) \land T(s_0, s_1) \land \neg I(s_1)]$

1: terminate? $S_C^1 = S_N^1 \quad \forall s_0, s_1[I(s_0) \land T(s_0, s_1) \rightarrow I(s_1)]$

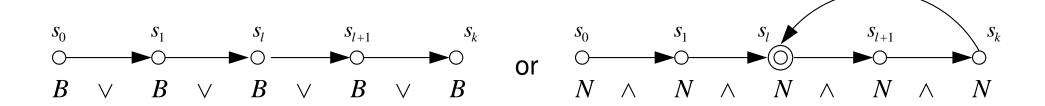
1: bad state? $B \cap S_N^1 \neq \emptyset$ $\exists s_0, s_1[I(s_0) \land T(s_0, s_1) \land B(s_1)]$

2: continue? $S_C^2 \neq S_N^2 \quad \exists s_0, s_1, s_2[I(s_0) \land T(s_0, s_1) \land T(s_1, s_2) \land \neg (I(s_2) \lor \exists t_0[I(t_0) \land T(t_0, s_2)])]$

2: terminate? $S_C^2 = S_N^2 \quad \forall s_0, s_1, s_2[I(s_0) \land T(s_0, s_1) \land T(s_1, s_2) \rightarrow I(s_2) \lor \exists t_0[I(t_0) \land T(t_0, s_2)]]$

2: bad state? $B \cap S_N^1 \neq \emptyset$ $\exists s_0, s_1, s_2[I(s_0) \land T(s_0, s_1) \land T(s_1, s_2) \land B(s_2)]$

look only for counter example made of k states (the bound)



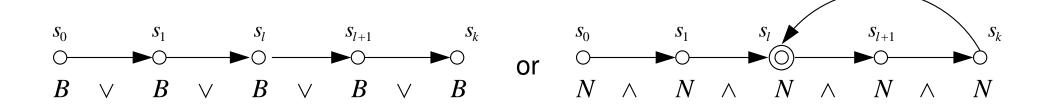
• simple for safety properties: bad state *B* is reachable

BMC(k):
$$I(s_0) \wedge T(s_0, s_1) \wedge \cdots \wedge T(s_{k-1}, s_k) \wedge \bigvee_{i=0}^k B(s_i)$$

harder for liveness properties cycle with no progress states N reachable

$$I(s_0) \wedge T(s_0, s_1) \wedge \cdots \wedge T(s_{k-1}, s_k) \wedge \bigwedge_{i=0}^k N(s_i) \wedge \exists l \ T(s_k, s_l)$$

 can also encode liveness into safety [BiereArthoSchuppan'01] • look only for counter example made of k states (the bound)



• simple for safety properties: bad state *B* is reachable

BMC(k):
$$I(s_0) \wedge T(s_0, s_1) \wedge \cdots \wedge T(s_{k-1}, s_k) \wedge \bigvee_{i=0}^k B(s_i)$$

harder for liveness properties cycle with no progress states N reachable

$$I(s_0) \wedge T(s_0, s_1) \wedge \cdots \wedge T(s_{k-1}, s_k) \wedge \bigwedge_{i=0}^k N(s_i) \wedge \bigvee_{l=0}^k T(s_k, s_l)$$

• can also encode liveness into safety [BiereArthoSchuppan'01]

- increase in efficiency of SAT solvers [Grasp,zChaff,MiniSAT,SatELite,...]
- SAT more robust than BDDs in bug finding
 (shallow bugs are easily reached by explicit model checking or testing)
- better unbounded but still SAT based model checking algorithms
 - k-induction [SinghSheeranStalmarck'00]
 - interpolation [McMillan'03]
- 4th Intl. Workshop on Bounded Model Checking (BMC'06)
- other logics, better encodings, e.g. [LatvalaBiereHeljankoJuntilla-FMCAD'04]
- other models, e.g. C/C++/Verilog [Kröning...], hybrid automata [Audemard...-BMC'04]

[SinghSheeranStalmarck'00]

- more specifically *k*-induction
 - does there exist k such that the following formula is unsatisfiable

$$\overline{B(s_0)} \wedge \cdots \wedge \overline{B(s_{k-1})} \wedge T(s_0, s_1) \wedge \cdots \wedge T(s_{k-1}, s_k) \wedge B(s_k) \wedge \bigwedge_{0 \le i < j \le k} s_i \ne s_j$$

- if *unsatisfiable* and BMC(k) *unsatisfiable* then bad state unreachable
- bound on k: length of longest cycle free path = reoccurrence diameter
- k = 0 check whether $\neg B$ tautological (propositionally)
- k = 1 check whether $\neg B$ inductive for T

- SAT based technique to overapproximate frontiers $Img(S_C)$
 - currently most effective technique to show that bad states are unreachable
 - better than BDDs and k-induction in many cases [HWMCC'08]
- starts from a resolution proof refutation of a BMC problem with bound k+1

$$S_C(s_0) \wedge T(s_0, s_1) \wedge T(s_1, s_2) \wedge \cdots \wedge T(s_k, s_{k+1}) \wedge B(s_{k+1})$$

- result is a characteristic function $f(s_1)$ over variables of the second state s_1
- these states do not reach the bad state s_{k+1} in k steps
- any state reachable from S_C satisfies f: $S_C(s_0) \land T(s_0, s_1) \Rightarrow f(s_1)$
- k is bounded by the diameter (exponentially smaller than longest cycle free path)

Chapter 14 on BMC in Handbook of Satisfiability

 $A \wedge B$ unsatisfiable then f is an interpolant iff

(I1)
$$A \Rightarrow f$$
 and (I2) $B \land f \Rightarrow \bot$

an interpolating quadruple (A,B) c[f] is well formed if

$$(\operatorname{W1}) \quad V(c) \subseteq V(A) \cup V(B) \qquad \text{and} \qquad (\operatorname{W2}) \quad V(f) \subseteq G \cup V(c) \qquad \text{with } G = V(A) \cap V(B)$$

an interpolating quadruple
$$(A,B)$$
 c $[f]$ is valid if
$$(V1) \quad A \Rightarrow f \qquad \text{and} \qquad (V2) \quad B \land f \Rightarrow c$$

proof rules which produce well formed and valid interpolating quadruples:

$$(\mathsf{R1}) \quad \frac{(A,B)\; c\; \dot{\lor}\; l\; [f] \quad (A,B)\; d\; \dot{\lor}\; \bar{l}\; [g]}{(A,B)\; c\; \lor d\; [f\wedge g]} \quad |l| \in V(B) \quad \quad (\mathsf{R3})$$

(R2)
$$\frac{(A,B) c \dot{l}[f] (A,B) d \dot{l}[g]}{(A,B) c \vee d [f|_{\bar{l}} \vee g|_{\bar{l}}]} |l| \not\in V(B) \quad (R4)$$

- through abstract interpretation resp. static analysis, or alternatively
- randomly simulate model and extract potential invariants
 - signals / predicates which always hold
 - implications of signals / predicates that occur in the simulation / tests
 - equivalent signals (works well in sequential equivalence checking)
- prove them to be *k*-inductive
 - quite natural in sequential equivalence checking for circuits
 - synthesis algorithms also only see finitely many time steps
- how to obtain environment model / constraints / contracts?

- inductive invariants help to speed-up both *k*-induction (and interpolation)
- let P be inductive: $I(s) \Rightarrow P(s)$ and $T(s,s') \land P(s) \Rightarrow P(s')$
- we want to prove that a bad state can not reached
- if BMC(k) is *unsatisfiable* it is enough to prove *unsatisfiability* of

$$P(s_0) \land P(s_1) \land \cdots \land P(s_k) \land \\ \overline{B(s_0)} \land \cdots \land \overline{B(s_{k-1})} \land \\ T(s_0, s_1) \land \cdots \land T(s_{k-1}, s_k) \land B(s_k) \land \bigwedge_{0 \le i < j \le k} s_i \ne s_j$$

• this formula can become *unsatisfiable* much earlier, i.e. for smaller k, than

$$\overline{B(s_0)} \wedge \cdots \wedge \overline{B(s_{k-1})} \wedge T(s_0, s_1) \wedge \cdots \wedge T(s_{k-1}, s_k) \wedge B(s_k) \wedge \bigwedge_{0 \le i < j \le k} s_i \ne s_j$$

[BiereBrummayer-FMCAD'08]

bounded model checking: [BiereCimattiClarkeZhu'99]

$$I(s_1) \wedge T(s_1, s_2) \wedge \ldots \wedge T(s_{k-1}, s_k) \wedge \bigvee_{0 \leq i \leq k} B(s_i)$$
 satisfiable?

• reoccurrence diameter checking: [BiereCimattiClarkeZhu'99]

$$T(s_1, s_2) \wedge \ldots \wedge T(s_{k-1}, s_k) \wedge \bigwedge_{1 \leq i < j \leq k} s_j$$
 unsatisfiable?

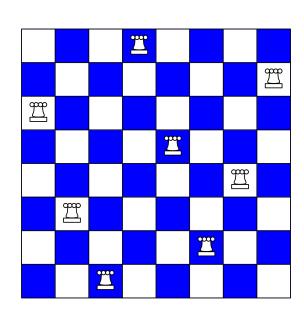
• *k*-induction base case: [SheeranSinghStålmarck'00]

$$I(s_1) \wedge T(s_1, s_2) \wedge \ldots \wedge T(s_{k-1}, s_k) \wedge B(s_k) \wedge \bigwedge_{0 \leq i < k} \neg B(s_i)$$
 satisfiable?

• *k*-induction induction step: [SheeranSinghStålmarck'00]

$$T(s_1, s_2) \wedge \ldots \wedge T(s_{k-1}, s_k) \wedge \underset{0 \leq i < k}{B(s_k)} \wedge \underset{1 \leq i < j \leq k}{\bigwedge} s_i \neq s_j$$
 unsatisfiable?

- classical concept in constraint programming:
 - -k variables over a domain of size m supposed to have different values
 - for instance k-queen problem
- propagation algorithms to establish arc-consistency
 - explicit propagators: [Régin'94]
 - * $O(k \cdot m)$ space
 - * $O(k^2 \cdot m^2)$ time



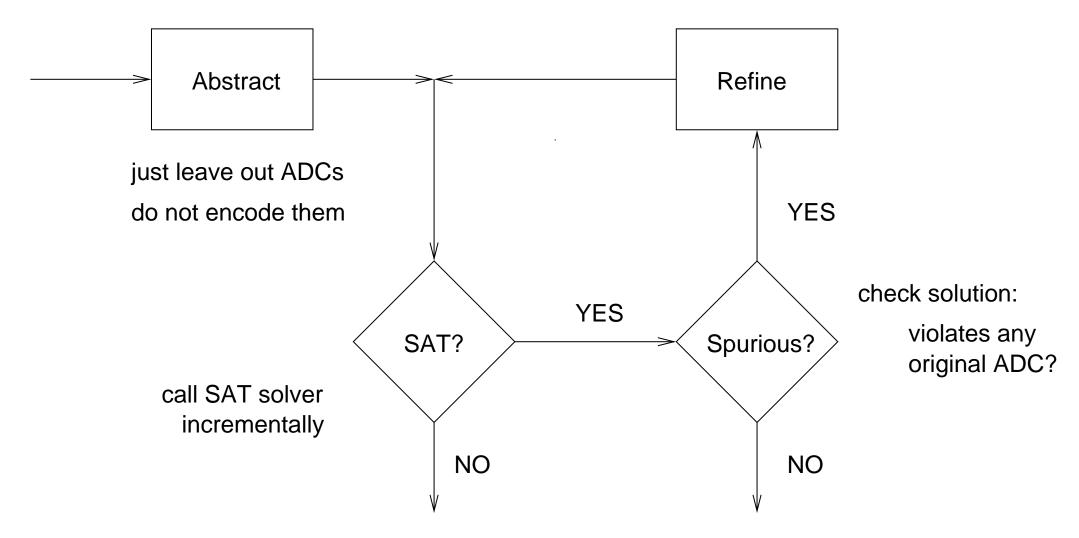
- symbolic propagators: [GentNightingale'04] also [MarquesSilvaLynce'07]
 - * one-hot CNF encoding with $\Omega(k \cdot m)$ boolean variables
- k < 1000 $m = 2^n > 2^{100}$ • in model checking $k \ll m$ typically n latches

encoding bit-vector inequalities directly:

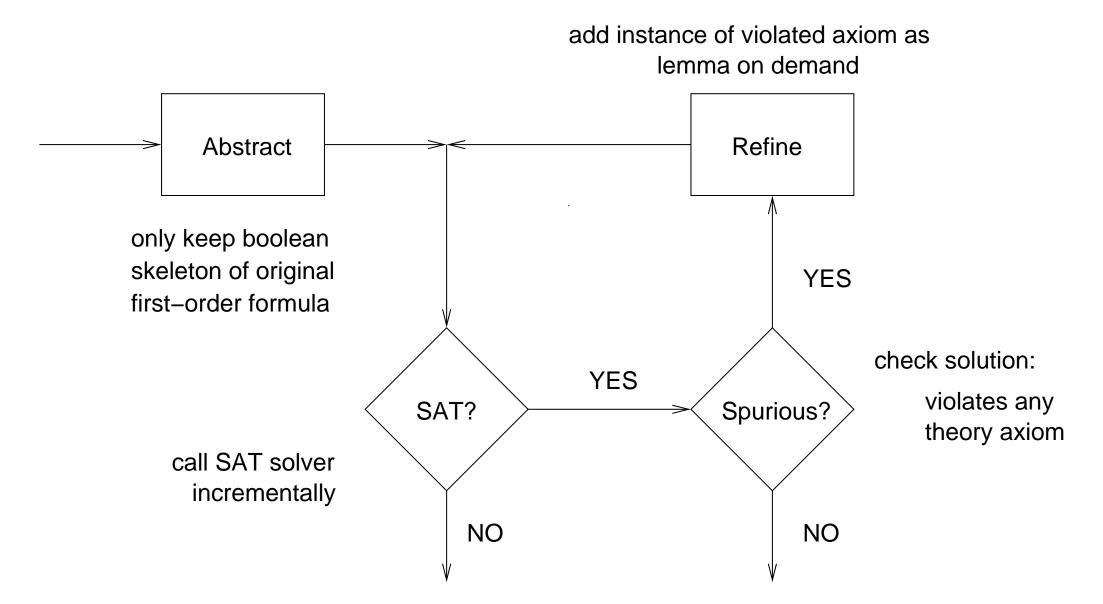
- let u, v be two *n*-bit vectors, d_0, \dots, d_{n-1} fresh boolean variables $(d_0 \vee \cdots \vee d_{n-1}) \wedge \bigwedge (u_j \vee v_j \vee \overline{d_j}) \wedge (\overline{u_j} \vee \overline{v_j} \vee \overline{d_j})$ $u \neq v$ is equisatisfiable to
- Ackermann Constraints + McCarthy Axioms can be extended to encode
- either eagerly encode all $s_i \neq s_i$ quadratic in k
- or refine adding bit-vector inequalities on demand [EénSörensson-BMC'03]
- natively handle ADCs within SAT solver: main contribution in FMCAD'08
 - similar to theory consistency checking in lazy SMT vs. "lemmas on demand"
 - can be extended to also perform theory propagation
- sorting networks ineffective in our experience [KröningStrichman'03,JussilaBiere'06]

TIP [EénSörensson-BMC'03]

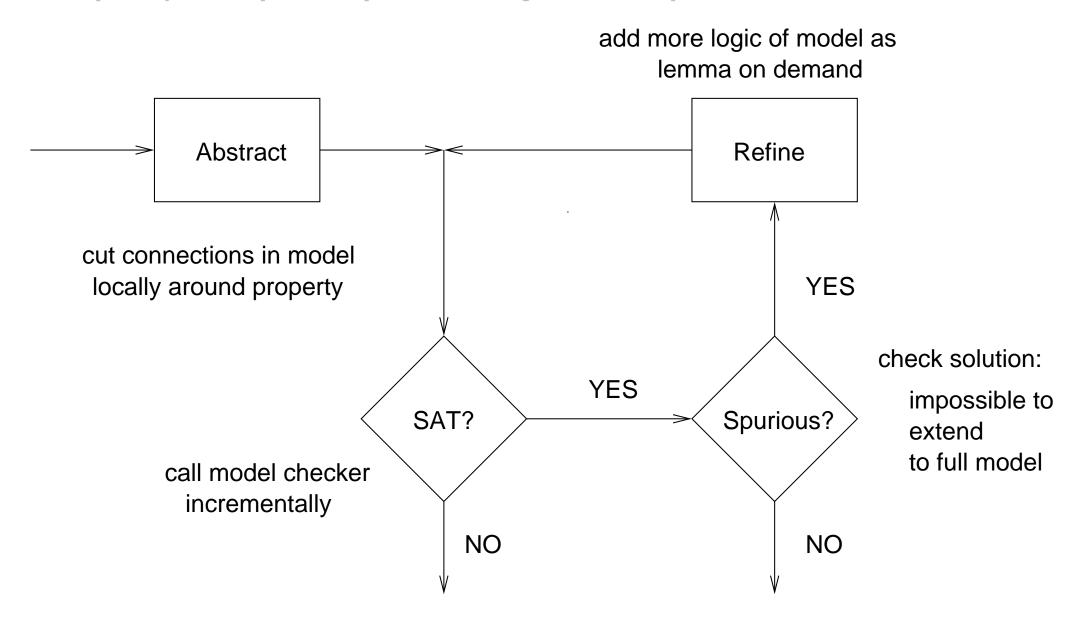
add violated ADC(s) as Lemma on Demand

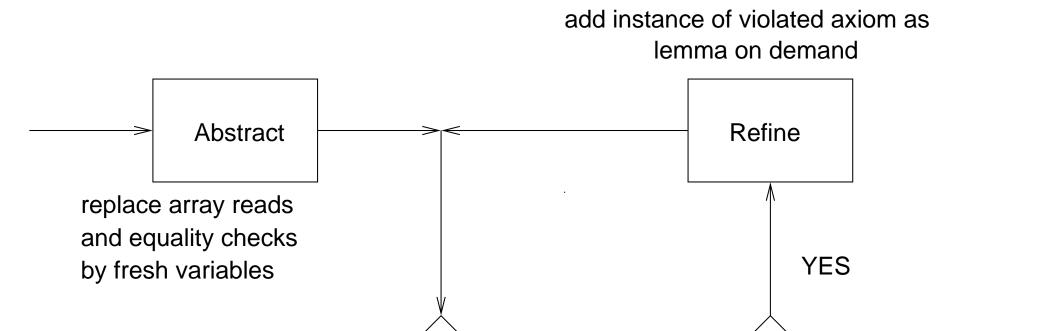


[DeMouraRueß-SAT'02] [BarrettDillStump-CAV'02] ...



Localization [Kurshan'93], Predicate Abstraction [GrafSaidi'97], SLAM [BallRajamani'01], CEGAR [ClarkeGrumbergJhaLuVeith'03]





SAT?

NO

YES

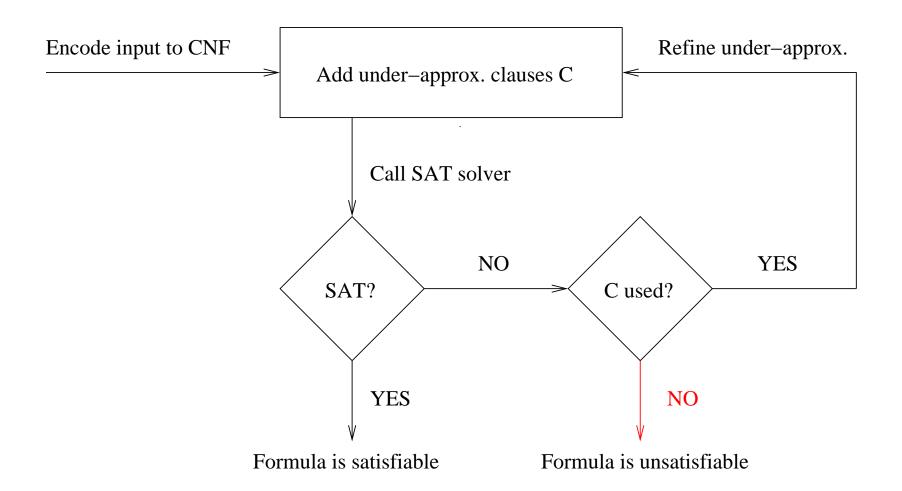
Spurious?

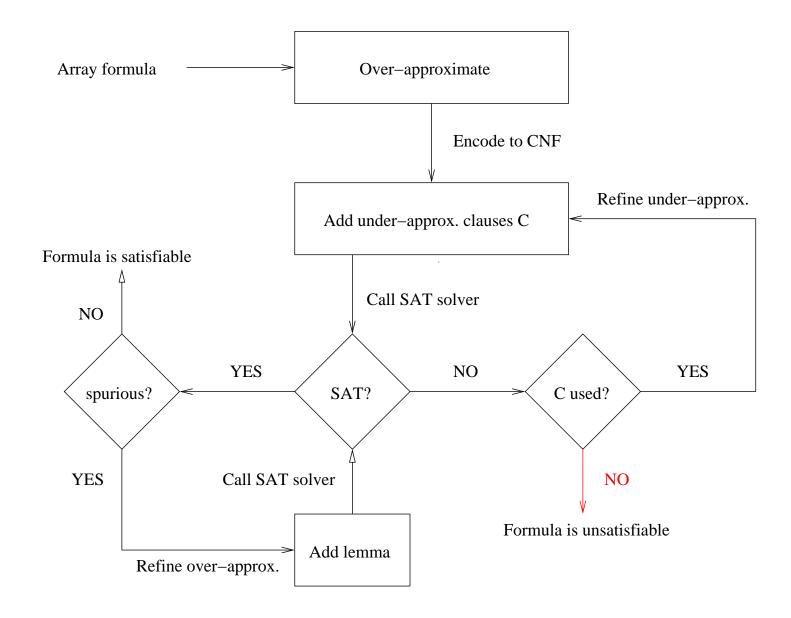
NO

call SAT solver incrementally check solution: violates any

array axiom

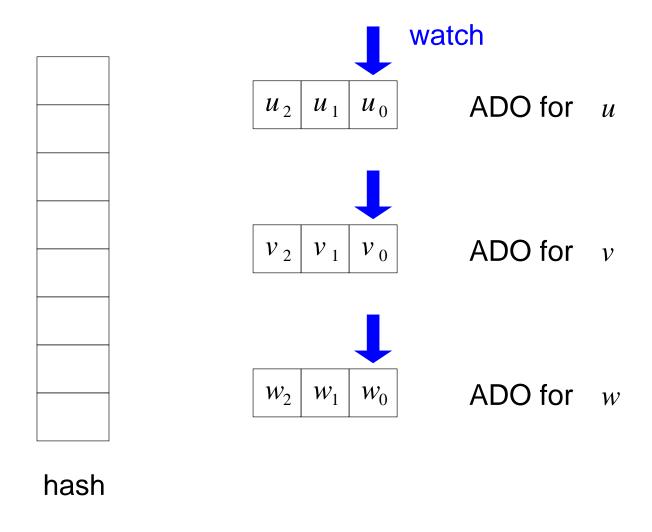
[BrummayerBiere-EuroCAST'09]



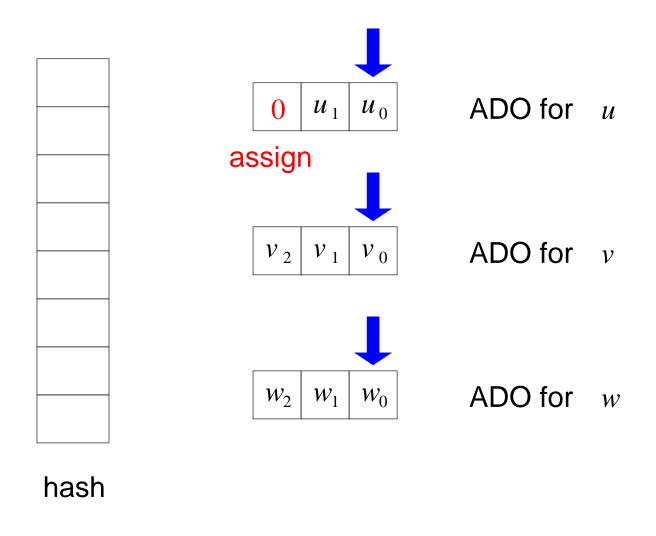


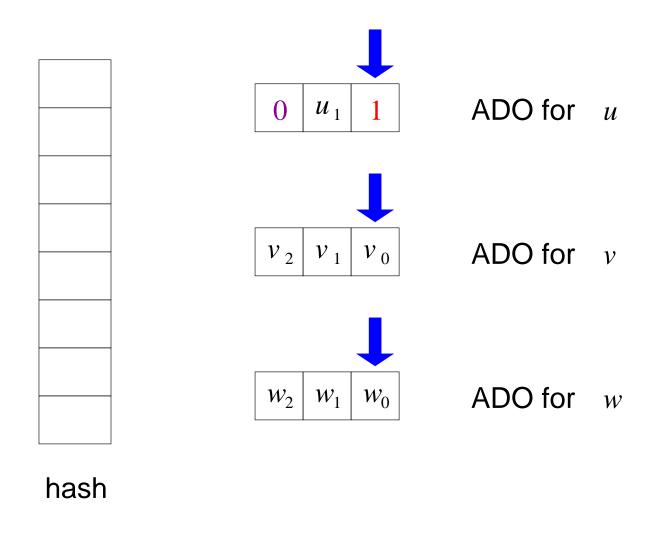
- Lemmas on Demand are as lazy as it gets
 - SAT solver enumerates full models of propositional skeleton
 - abstracted lemmas are added / learned on demand
 - theory solver checks consistency of conjunction of theory literals
- on-the-fly consistency checking
 - additionally theory solver checks consistency of partial model as well
- theory propagation
 - theory solver even deduces and notifies SAT solver about implied values of literals
- generic framework: DPLL(T) [NieuwenhuisOliverasTinelli-JACM'06]

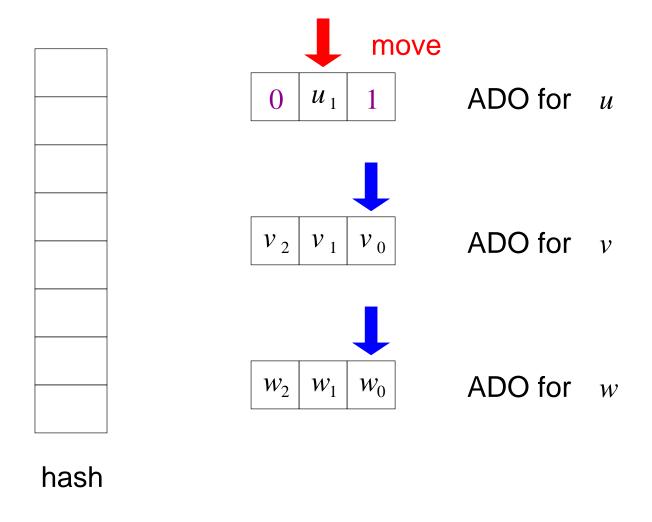
[BiereBrummayer-FMCAD'08]

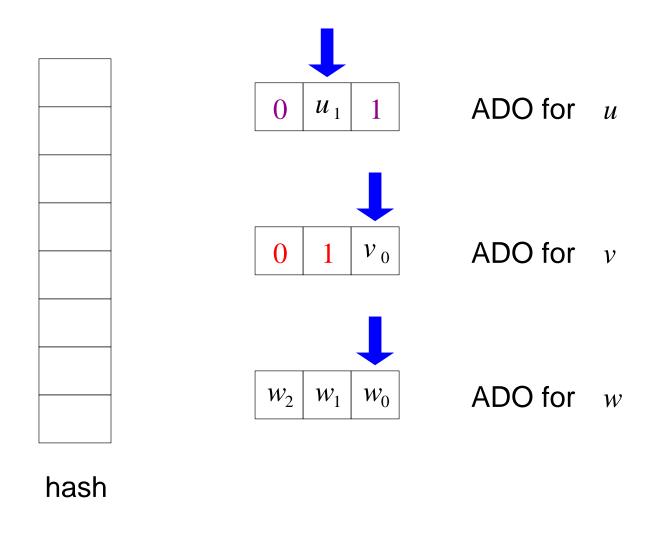


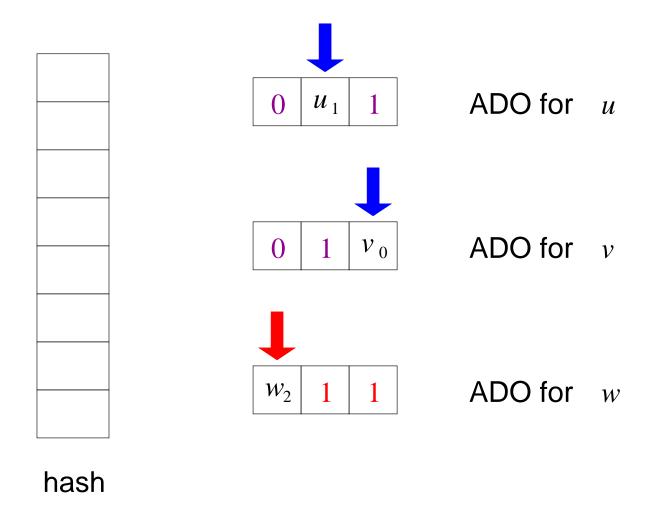
[BiereBrummayer-FMCAD'08]

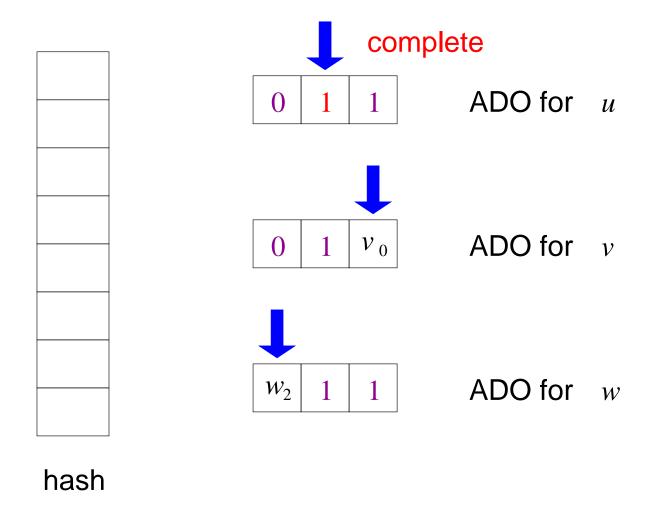


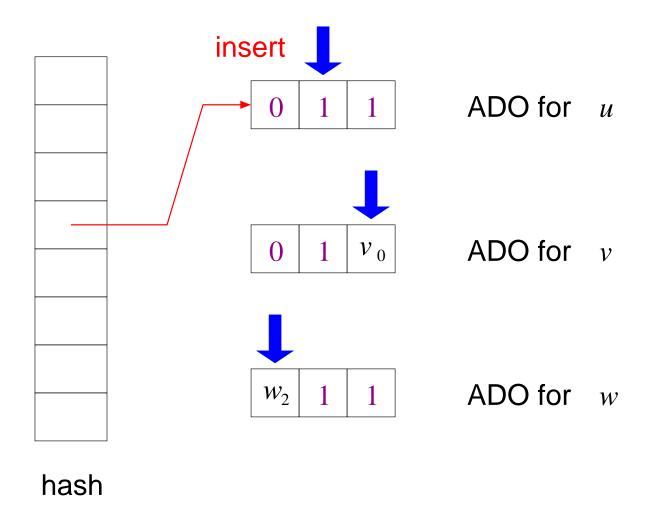


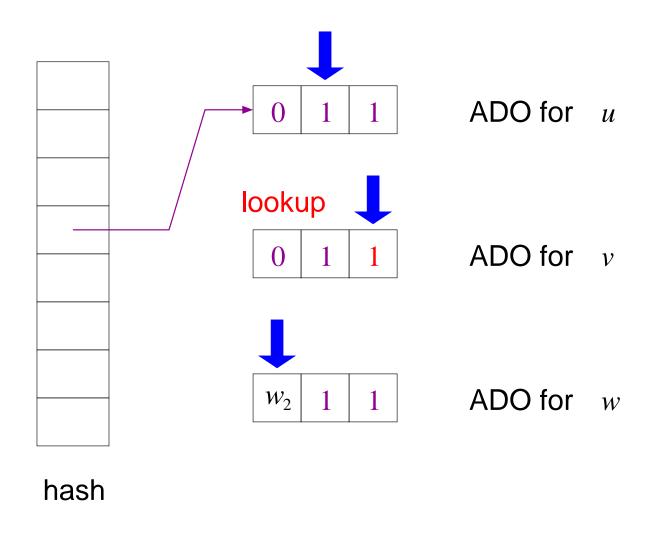


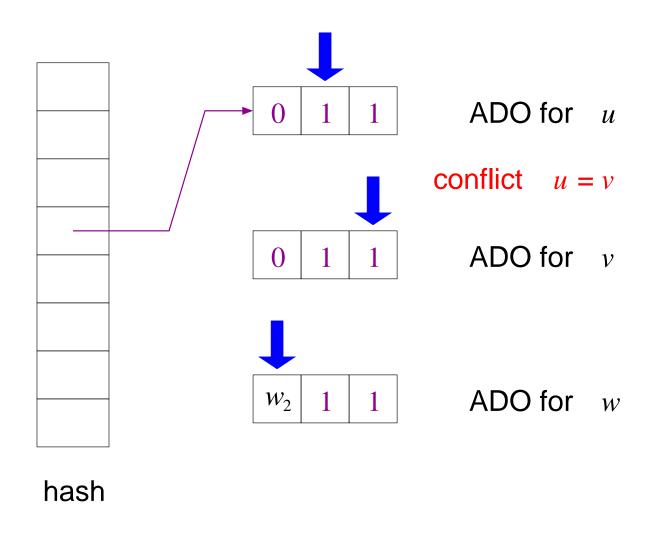






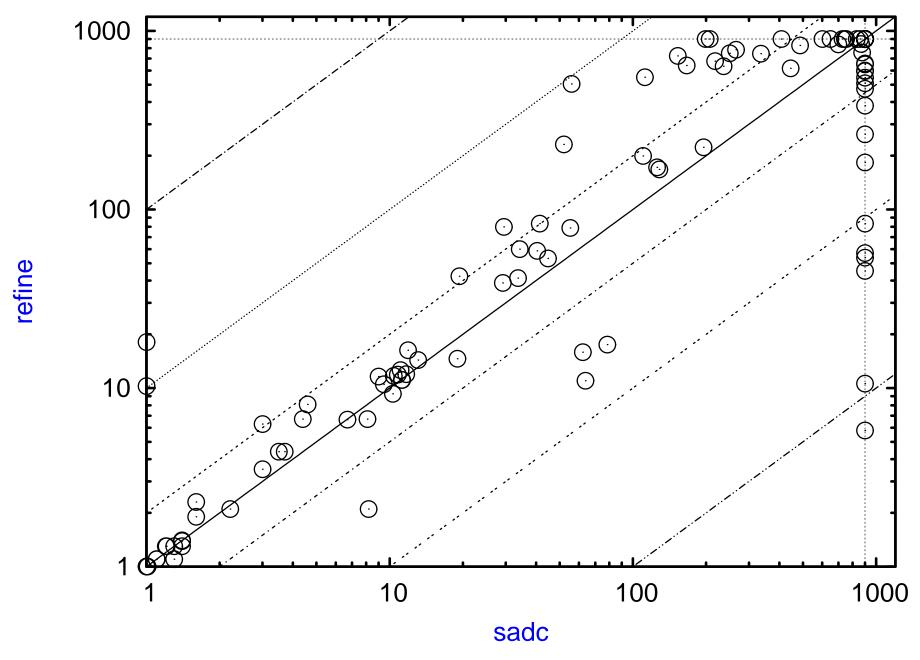


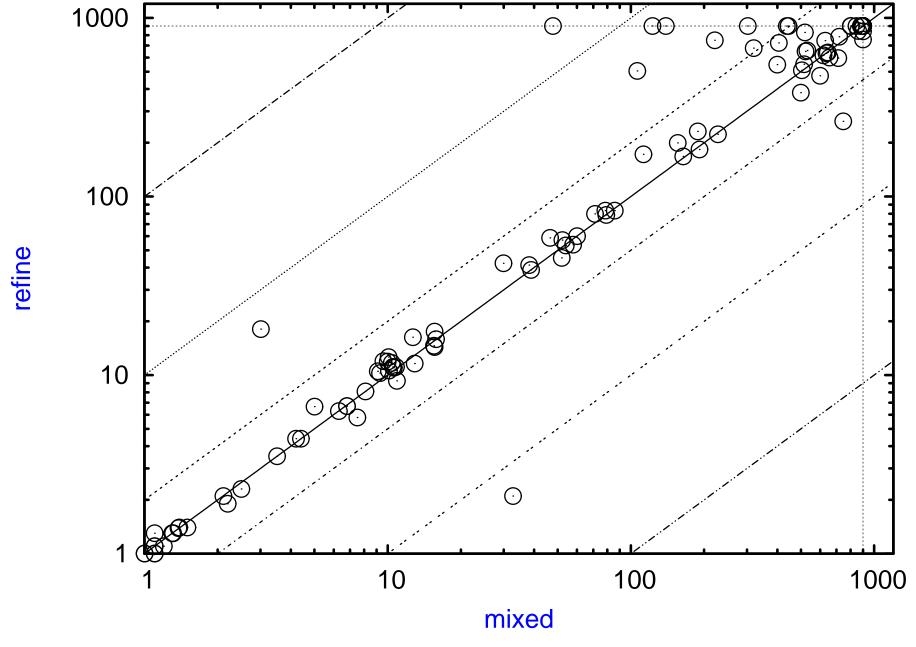




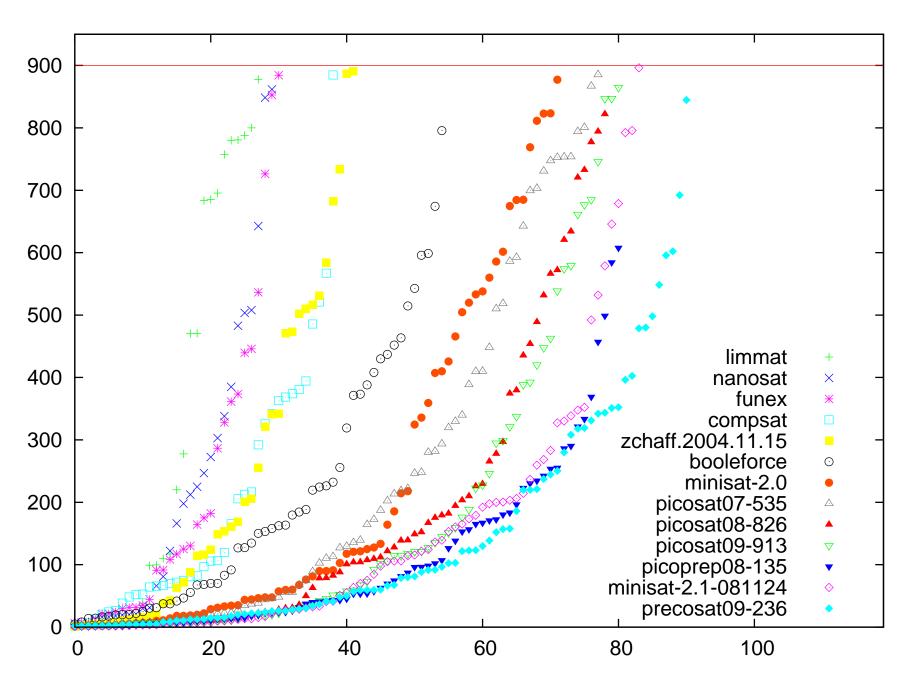
- ADO key is calculated from concrete bit-vector
 - by for instance XOR'ing bits word by word
- ADOs watched by variables (not literals)
 - during backtracking all inserted ADOs need to be removed from hash table
 - save whether variable assignment forced ADO to be inserted
 - stack like insert/remove operations on hash table allow open addressing
- conflict analysis
 - all bits of the bit-vectors in conflict are followed
 - can be implemented by temporarily generating a pseudo clause

$$(u_2 \vee \overline{u}_1 \vee \overline{u}_0 \vee v_2 \vee \overline{v}_1 \vee \overline{v}_0)$$





- symbolic consistency checker for ADCs over bit-vectors
 - successfully applied to simple path constraints in model checking
 - similar to theory consistency checking in lazy SMT solvers
 - combination with eager refinement approach
 lemmas on demand
- future work: ADC based BCP for bit-vectors
 - aka theory propagation in lazy SMT solvers
 - extensions to handle Ackermann constraints or even McCarthy axioms
 - one-way to get away from pure bit-blasting in BV



Introduction to Bounded Model Checking - FATS Seminar ETH 2009

- bounded model checking
 - routinely used in HW industry for falsification
 - need to improve word-level techniques for SW and HW verification / falsification
- SAT (and SMT) has seen tremendous improvements in recent years
 - was key enabler to make bounded model checking successful
 - many applications through the whole field of computer science
- still lots of opportunities:
 - parallel Model Checking / parallel SMT and SAT solving
 - portfolio and preprocessing (PrecoSAT was our first attempt)
 - make quantified boolean formula (QBF) reasoning work (QBF is PSPACE compl.)